--- 2018 Multimaster RSRC "ma" VHDL Code

--- Current file name: ma.vhd

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LIBRARY IEEE ;

USE IEEE.STD\_LOGIC\_1164.ALL ;

ENTITY ma IS

PORT (bus\_in : IN STD\_LOGIC\_VECTOR(31 DOWNTO 0) ;

address : OUT STD\_LOGIC\_VECTOR(31 DOWNTO 0) ;

clk : IN STD\_LOGIC ;

grant : IN STD\_LOGIC ;

ma\_in : IN STD\_LOGIC) ;

END ma ;

ARCHITECTURE behavioral OF ma IS

SIGNAL address\_int : STD\_LOGIC\_VECTOR(31 DOWNTO 0) ;

BEGIN

mareg:PROCESS(clk)

BEGIN

IF (clk = '1' AND clk'EVENT) THEN

IF (ma\_in = '1') THEN

address\_int(31 DOWNTO 0 ) <= bus\_in(31 DOWNTO 0) ;

END IF ;

END IF ;

END PROCESS mareg ;

pindrive:PROCESS(grant,address\_int)

BEGIN

IF (grant = '1') THEN

address <= address\_int ;

ELSE

address <= (OTHERS => 'Z') ;

END IF ;

END PROCESS pindrive ;

END behavioral ;